

SD2943 model based on 2 x SD2941-10 model + series Gate
Resistors

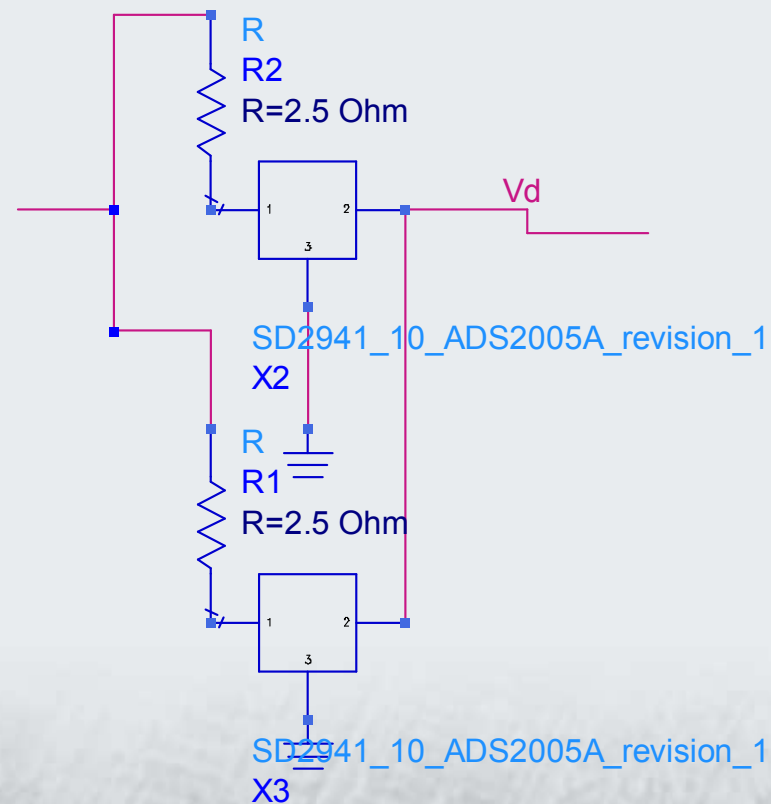


Quakertown , PA

Qtn-jp-218-rev0

January 3 , 2008

SD2943 model using SD2941-10 model + Series Gate resistance

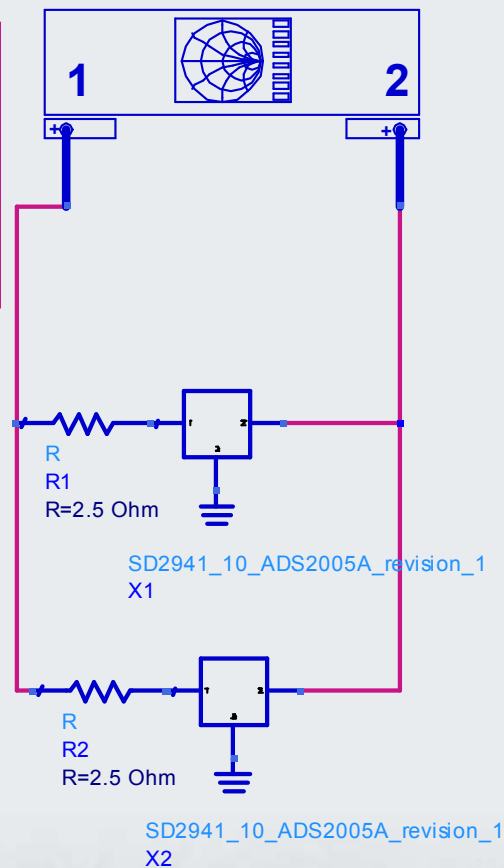


SET frequency Start / Stop
Set Gate Voltage = VBias1
SET Drain Voltage = VBias2

SP_NWA
SP_NWA1
Start=50 MHz
Stop=200 MHz
NumPoints=16
VBias1=3.6
VBias2=50
Port1Z=50
Port2Z=50

S_StabCircle
S_StabCircle1
S_StabCircle1=s_stab_circle(S,51)

L_StabCircle
L_StabCircle1
L_StabCircle1=l_stab_circle(S,51)



STMicroelectronics
ADS2005A
RF Small Signal template revision 0
John Pritiskutch_ST_Quakertown
March 30 2006

StabFact
StabFact1
StabFact1=stab_fact(S)

MaxGain
MaxGain1
MaxGain1=max_gain(S)

Example of ADS schematic



Example of S-parameter analysis

freq	S(1,1)	S(2,1)	S(1,2)	S(2,2)
50.00 MHz	0.911 / -179.219	2.926 / 73.201	0.003 / 35.568	0.938 / -178.789
60.00 MHz	0.912 / -179.208	2.391 / 70.081	0.003 / 42.381	0.940 / -178.696
70.00 MHz	0.914 / -179.199	2.005 / 67.107	0.003 / 48.756	0.943 / -178.614
80.00 MHz	0.915 / -179.196	1.712 / 64.286	0.003 / 54.549	0.945 / -178.549
90.00 MHz	0.917 / -179.202	1.483 / 61.623	0.004 / 59.676	0.948 / -178.503
100.0 MHz	0.919 / -179.217	1.298 / 59.120	0.004 / 64.121	0.951 / -178.473
110.0 MHz	0.920 / -179.241	1.147 / 56.774	0.004 / 67.917	0.954 / -178.461
120.0 MHz	0.922 / -179.274	1.021 / 54.584	0.005 / 71.127	0.956 / -178.463
130.0 MHz	0.924 / -179.315	0.914 / 52.544	0.005 / 73.824	0.959 / -178.478
140.0 MHz	0.925 / -179.362	0.824 / 50.649	0.006 / 76.083	0.961 / -178.505
150.0 MHz	0.926 / -179.414	0.745 / 48.892	0.006 / 77.973	0.963 / -178.541
160.0 MHz	0.928 / -179.472	0.678 / 47.267	0.007 / 79.554	0.965 / -178.584
170.0 MHz	0.929 / -179.533	0.619 / 45.766	0.007 / 80.880	0.967 / -178.635
180.0 MHz	0.930 / -179.598	0.567 / 44.383	0.007 / 81.994	0.969 / -178.690
190.0 MHz	0.931 / -179.665	0.521 / 43.112	0.008 / 82.931	0.971 / -178.750
200.0 MHz	0.932 / -179.734	0.481 / 41.945	0.008 / 83.722	0.972 / -178.812



Example of S-parameter analysis

